ABSTRACT

It is a general object of the present invention to provide an improved method of fabrication in the formation of an improved copper metal diffusion barrier layer having the structure, W/WSiN/WN, in single and dual damascene interconnect trench/contact via processing with 0.10 micron nodes for MOSFET and CMOS applications. The diffusion barrier is formed by depositing a tungsten nitride bottom layer, followed by an in situ SiH_4/NH_3 or SiH_4/H_2 soak forming a WSiN layer, and depositing a final top layer of tungsten. This invention is used to manufacture reliable metal interconnects and contact vias in the fabrication of MOSFET and CMOS devices for both logic and memory applications and the copper diffusion barrier formed, W/WSiN/WN, passes a stringent barrier thermal reliability test at 400 °C. Pure single barrier layers, i.e., single layer WN, exhibit copper punch through or copper spiking during the stringent barrier thermal reliability test at 400 °C.